WHAT IS CLAIMED IS:

1. A method for testing semiconductor devices that output non-deterministic entity information, the method including the steps:

generating test signals with a semiconductor tester;

applying the generated test signals to the device-under-test;

capturing actual output entities from the DUT in response to the applied generated test signals;

comparing the actual output entities to expected output entities and identifying a fail condition where a comparison fails to match an actual output entity to an expected output entity; and

if a failure is identified in the comparing step, defining a window of valid expected entities and comparing the failed actual output entity to the window of valid expected entities.

2. A method according to claim 1 and further including the step:

substituting the fail condition with a pass condition where further comparing the failed actual output entity to the window of valid expected entities leads to a match between the failed actual output entity and any one of the valid expected entities in the window.

3. A method according to claim 1 wherein the generating test signals includes:

creating a bus layout file.

4. A method according to claim 3 wherein the creating a bus layout file includes:

identifying the device complexity.

5. A method according to claim 1 wherein the step of generating test signals includes:

producing a list of packet and control entities.

6. A method according to claim 1 wherein each entity comprises a packet or control signal according to a serial or parallel communications protocol.

7. A method according to claim 4 wherein the step of defining a window includes:

establishing a range of valid entities for the actual entities to fall within based upon the device complexity and typeorder.

8. Automatic test equipment for testing semiconductor devices that output non-deterministic entity information, the automatic test equipment including:

means for generating test signals;

means for applying the generated test signals to the device-under-test;

means for capturing actual output entities from the DUT in response to the applied generated test signals;

means for comparing the actual output entities to expected output entities and identifying a fail condition where a comparison fails to match an actual output entity to an expected output entity; and

if a failure is identified in the comparing step, means for defining a window of valid expected entities and comparing the failed actual output entity to the window of valid expected entities.

9. Automatic test equipment according to claim 8 and further including:

means for substituting the fail condition with a pass condition where further comparing the failed actual output entity to the window of valid expected entities leads to a match between the failed actual output entity and any one of the valid expected entities in the window.

10. A computer-readable medium having stored thereon sequences of instructions which, when executed, cause one or more electronic systems to carry out the steps:

generating test signals with a semiconductor tester;

applying the generated test signals to the device-under-test;

capturing actual output entities from the DUT in response to the applied generated test signals;

comparing the actual output entities to expected output entities and identifying a fail condition where a comparison fails to match an actual output entity to an expected output entity; and

if a failure is identified in the comparing step, defining a window of valid expected entities and comparing the failed actual output entity to the window of valid expected entities.